



Fault-Protected, 12-Bit ADCs with Software-Selectable Input Range

MAX1272/MAX1273

General Description

The MAX1272/MAX1273 multirange 12-bit data-acquisition systems (DAS) operate with a single 5V supply. The software-programmable analog input accepts a variety of voltage ranges: $\pm 10V$, $\pm 5V$, 0 to 10V, 0 to 5V for the MAX1272; $\pm V_{REF}$, $\pm V_{REF} / 2$, 0 to V_{REF} , 0 to $V_{REF} / 2$ for the MAX1273. The software-selectable extended analog input range increases the effective dynamic range to 14 bits and provides the flexibility to interface 4–20mA powered sensors directly to a single 5V system. In addition, the MAX1272 provides fault protection to $\pm 12V$. Other features include a 5MHz track/hold (T/H) bandwidth, 87ksps throughput rate, and internal (4.096V) or external (2.40V to 4.18V) reference.

The MAX1272/MAX1273 serial interfaces connect directly to SPI™/QSPI™/MICROWIRE™-compatible devices without any external logic.

Four software-programmable power-down modes (delayed standby, immediate standby, delayed full power-down, and immediate full power-down) provide low-current shutdown between conversions. In standby mode, the internal reference buffer remains active, thus eliminating startup delay.

The MAX1272/MAX1273 are available in an 8-pin PDIP package. Both devices are available in the commercial (0°C to +70°C) or extended (-40°C to +85°C) temperature range.

Applications

- Industrial Control Systems
- Data-Acquisition Systems
- Robotics
- Automatic Testing
- Battery-Powered Instruments
- Medical Instruments

Typical Application Circuit appears at end of data sheet.

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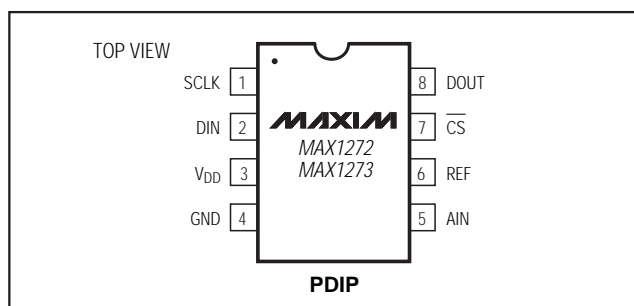
Features

- ◆ **Four Software-Selectable Input Ranges**
 MAX1272: 0 to 10V, 0 to 5V, $\pm 10V$, $\pm 5V$
 MAX1273: 0 to V_{REF} , 0 to $V_{REF} / 2$, $\pm V_{REF}$, $\pm V_{REF} / 2$
- ◆ **12-Bit Resolution, No Missing Codes**
- ◆ **5V Single-Supply Operation**
- ◆ **SPI/QSPI/MICROWIRE-Compatible 3-Wire Interface**
- ◆ **87ksps Sampling Rate**
- ◆ **$\pm 12V$ Fault-Protected Analog Input (MAX1272)**
- ◆ **Internal (4.096V) or External (2.4V to 4.18V) Reference**
- ◆ **Low Power**
 1.5mA at 87ksps
 0.4mA at 10ksps
 0.2mA at 1ksps
- ◆ **Four Power-Down Modes**
- ◆ **8-Pin PDIP Package**

Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE | INL (LSB) |
|------------|----------------|---------------|-----------|
| MAX1272CPA | 0°C to +70°C | 8 Plastic DIP | ± 1 |
| MAX1272EPA | -40°C to +85°C | 8 Plastic DIP | ± 1 |
| MAX1273CPA | 0°C to +70°C | 8 Plastic DIP | ± 1 |
| MAX1273EPA | -40°C to +85°C | 8 Plastic DIP | ± 1 |

Pin Configuration



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ABSOLUTE MAXIMUM RATINGS

| | |
|---|-----------------------------------|
| V _{DD} to GND | -0.3V to +6V |
| AIN to GND (MAX1272) | ±12V |
| AIN to GND (MAX1273) | ±6V |
| DOUT, CS, DIN, SCLK, REF to GND | -0.3V to (V _{DD} + 0.3V) |
| Maximum Current into Any Pin | 50mA |
| Continuous Power Dissipation (T _A = +70°C) | |
| 8-Pin Plastic DIP (derate 9.1mW/°C above +70°C) | 727mW |

Operating Temperature Ranges

| | |
|---|-----------------|
| MAX127_CPA | 0°C to +70°C |
| MAX127_EPA | -40°C to +85°C |
| Storage Temperature Range | -65°C to +150°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Junction Temperature | +150°C |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 4.75V to 5.25V, unipolar/bipolar input range, external reference mode, V_{REF} = 4.096V, C_{REF} = 1.0μF, f_{SCLK} = 1.4MHz, 50% duty cycle, C_{LOAD} = 50pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

| PARAMETERS | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|------------------|-----------------------------------|-----|-------|-------|--------|
| ACCURACY (Note 1) | | | | | | |
| Resolution | | | 12 | | | Bits |
| Integral Nonlinearity | INL | | | ±0.3 | ±1.0 | LSB |
| Differential Nonlinearity | DNL | No missing codes over temperature | | ±0.35 | ±1.00 | LSB |
| Offset Error | | Unipolar | | | ±5 | LSB |
| | | Bipolar | | | ±10 | |
| Gain Error (Note 2) | | Unipolar | | | ±10 | LSB |
| | | Bipolar | | | ±10 | |
| Gain Error Temperature Coefficient (Note 2) | | Unipolar | | | ±3 | ppm/°C |
| | | Bipolar | | | ±5 | |
| DYNAMIC SPECIFICATIONS (10kHz sine-wave input, ±10V_{P-P} (MAX1272), or ±4.096V_{P-P} (MAX1273), f_{SAMPLE} = 87ksps) | | | | | | |
| Signal-to-Noise + Distortion Ratio | SINAD | | 69 | 72 | | dB |
| Total Harmonic Distortion | THD | Up to the 5th harmonic | | -87 | -78 | dB |
| Spurious-Free Dynamic Range | SFDR | | 80 | 88 | | dB |
| Aperture Delay | t _{AD} | | | 15 | | ns |
| Aperture Jitter | t _{AJ} | | | <50 | | ps |
| ANALOG INPUT | | | | | | |
| T/H Acquisition Time | t _{ACQ} | | | | 2.85 | μs |

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ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 4.75V to 5.25V, unipolar/bipolar input range, external reference mode, V_{REF} = 4.096V, C_{REF} = 1.0μF, f_{SCLK} = 1.4MHz, 50% duty cycle, C_{LOAD} = 50pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

| PARAMETERS | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|--|---------------------|--|---------|---------------------------------|-----------------------|-----------------------|-------|
| Small-Signal Bandwidth | BW _{-3dB} | ±10V (MAX1272) or ±V _{REF} (MAX1273) range | | 5 | | MHz | |
| | | ±5V (MAX1272) or ±V _{REF} / 2 (MAX1273) range | | 2.5 | | | |
| | | 0 to 10V (MAX1272) or 0 to V _{REF} (MAX1273) range | | 2.5 | | | |
| | | 0 to 5V (MAX1272) or 0 to V _{REF} / 2 (MAX1273) range | | 1.25 | | | |
| Input Voltage Range (Tables 2, 3) | V _{IN} | Unipolar | MAX1272 | RNG = 1 | 0 | 10 | V |
| | | | | RNG = 0 | 0 | 5 | |
| | | | MAX1273 | RNG = 1 | 0 | V _{REF} | |
| | | | | RNG = 0 | 0 | V _{REF} / 2 | |
| | | Bipolar | MAX1272 | RNG = 1 | -10 | +10 | |
| | | | | RNG = 0 | -5 | +5 | |
| | | | MAX1273 | RNG = 1 | -V _{REF} | +V _{REF} | |
| | | | | RNG = 0 | -V _{REF} / 2 | +V _{REF} / 2 | |
| Input Current | I _{IN} | Unipolar | MAX1272 | 0 to 10V range | -10 | +860 | μA |
| | | | | 0 to 5V range | -10 | +430 | |
| | | | MAX1273 | 0 to V _{REF} range | -10 | +10 | |
| | | | | 0 to V _{REF} / 2 range | -10 | +10 | |
| | | Bipolar | MAX1272 | ±10V range | -1400 | +860 | |
| | | | | ±5V range | -720 | +430 | |
| | | | MAX1273 | ±V _{REF} range | -1400 | +10 | |
| | | | | ±V _{REF} / 2 range | -720 | +10 | |
| Input Capacitance | | | | 40 | | pF | |
| INTERNAL REFERENCE | | | | | | | |
| REF Output Voltage | V _{REF} | | | 4.036 | 4.096 | 4.156 | V |
| REF Output Tempco | TC V _{REF} | MAX127_C | | ±15 | | ppm/°C | |
| | | MAX127_E | | ±30 | | | |
| Output Short-Circuit Current | | REF shorted to GND | | 40 | | mA | |
| Load Regulation | | 0 to 0.5mA output current | | 0.7 | 10 | mV | |
| Capacitive Bypass at REF | | | | 1 | | μF | |
| REFERENCE INPUT (Reference buffer disabled, reference input applied to REF) | | | | | | | |
| Input Voltage Range | | | | 2.40 | | 4.18 | V |

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ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 4.75V to 5.25V, unipolar/bipolar input range, external reference mode, V_{REF} = 4.096V, C_{REF} = 1.0 μ F, f_{SCLK} = 1.4MHz, 50% duty cycle, C_{LOAD} = 50pF, T_A = T_{MIN} to T_{MAX} , unless otherwise noted. Typical values are at T_A = +25°C.)

| PARAMETERS | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|------------|---|-------------------------|-----|-----------|---------|
| Input Current | | V_{REF} = 4.096V | Converting | 400 | 850 | μ A |
| | | | Standby power-down mode | 5 | 10 | |
| | | | Full power-down mode | | 1 | |
| POWER REQUIREMENTS | | | | | | |
| Supply Voltage | V_{DD} | | 4.75 | 5 | 5.25 | V |
| Supply Current (Internal Reference Mode) | I_{DD} | Converting | Bipolar | 2.4 | 4 | mA |
| | | | Unipolar | 2.2 | 3 | |
| | | Standby power-down mode | 400 | 700 | μ A | |
| | | Full power-down mode | 1 | | | |
| Supply Current (External Reference Mode) | I_{DD} | Converting | Bipolar | 1.5 | 2.5 | mA |
| | | | Unipolar | 1.2 | 2.0 | |
| | | Standby power-down mode | 200 | 450 | μ A | |
| | | Full power-down mode | 1 | | | |
| Power-Supply Rejection Ratio (Note 3) | PSRR | External reference = 4.096V | ± 0.3 | | ± 1.0 | LSB |
| | | Internal reference | | | ± 0.5 | |
| TIMING | | | | | | |
| Clock Frequency Range | f_{SCLK} | | 0.1 | | 1.4 | MHz |
| T/H Acquisition Time | t_{ACQ} | (Note 4) | 2.85 | | | μ s |
| Conversion Time | t_{CONV} | (Note 4) | 8.57 | | | μ s |
| Throughput Rate | | | | | 87.5 | ksps |
| Internal Reference Settling Time | | REF bypass capacitor initially discharged | | 2 | | ms |
| Device Power-Up Time | | External reference mode | | 10 | | μ s |
| DIGITAL INPUTS (DIN, SCLK, and \overline{CS}) | | | | | | |
| Input High-Threshold Voltage | V_{IH} | | | | 2.4 | V |
| Input Low-Threshold Voltage | V_{IL} | | 0.8 | | | V |
| Input Hysteresis | V_{HYS} | | | 0.2 | | V |
| Input Leakage Current | I_{IN} | V_{IN} = 0 to V_{DD} | -10 | | +10 | μ A |
| Input Capacitance | C_{IN} | | | 15 | | pF |
| DIGITAL OUTPUT (DOUT) | | | | | | |
| Output Voltage Low | V_{OL} | I_{SINK} = 10mA | | | 0.4 | V |
| | | I_{SINK} = 16mA | | 0.6 | | |
| Output Voltage High | V_{OH} | I_{SOURCE} = 0.5mA | V_{DD} | | -0.5 | V |
| Three-State Leakage Current | I_L | \overline{CS} = V_{DD} | -10 | | +10 | μ A |
| Three-State Output Capacitance | C_{OUT} | \overline{CS} = V_{DD} | | 15 | | pF |

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TIMING CHARACTERISTICS

($V_{DD} = 4.75V$ to $5.25V$, unipolar/bipolar input range, external reference mode, $V_{REF} = 4.096V$, $C_{REF} = 1.0\mu F$, $f_{SCLK} = 1.4MHz$, 50% duty cycle, $C_{LOAD} = 50pF$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Figures 1 and 4)

| PARAMETERS | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-----------|------------|-----|-----|-----|-------|
| DIN to SCLK Setup | t_{DS} | | 100 | | | ns |
| DIN to SCLK Hold | t_{DH} | | | | 0 | ns |
| SCLK Fall to Output Data Valid | t_{DO} | | 20 | | 250 | ns |
| \overline{CS} Fall to Output Enable | t_{DV} | | | | 100 | ns |
| \overline{CS} Rise to Output Disable | t_{TR} | | | | 100 | ns |
| \overline{CS} to SCLK Rise Setup | t_{CSS} | | 100 | | | ns |
| \overline{CS} to SCLK Rise Hold | t_{CSH} | | 0 | | | ns |
| SCLK Pulse Width High | t_{CH} | | 200 | | | ns |
| SCLK Pulse Width Low | t_{CL} | | 200 | | | ns |

Note 1: Accuracy specifications tested at $V_{DD} = 5V$. Performance at power-supply tolerance limit is guaranteed by power-supply rejection test.

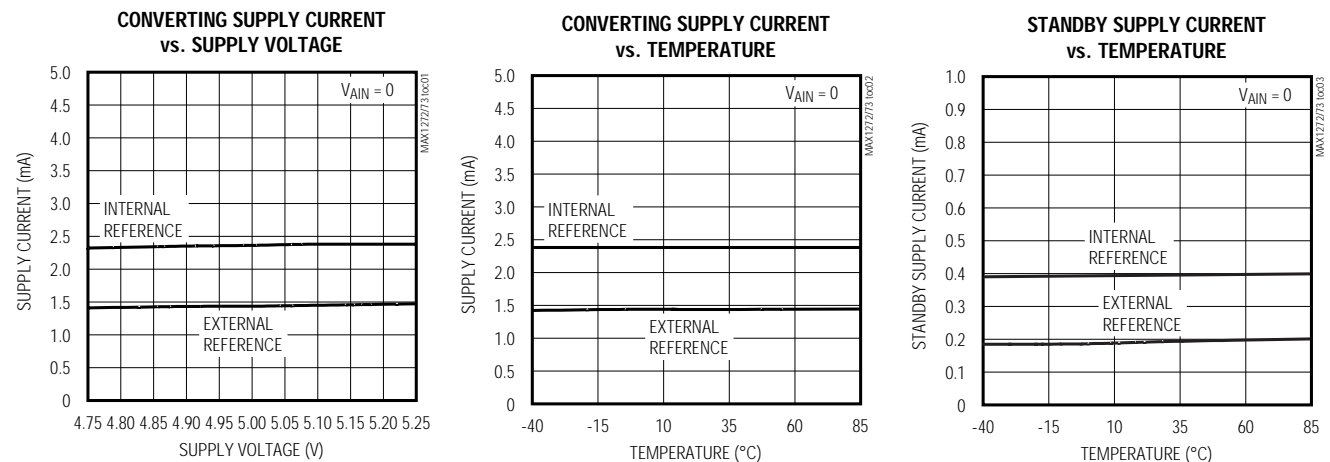
Note 2: Offset error nulled. The ideal last-code transition is (FS - 1.5 LSB).

Note 3: PSRR measured at full scale. Tested at $\pm 10V$ (MAX1272) and $\pm 4.096V$ (MAX1273) input ranges.

Note 4: Acquisition and conversion times are dependent on the clock speed.

Typical Operating Characteristics

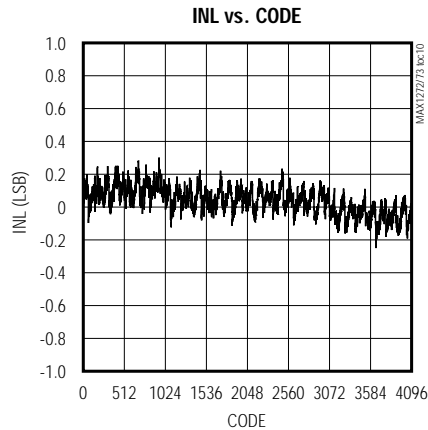
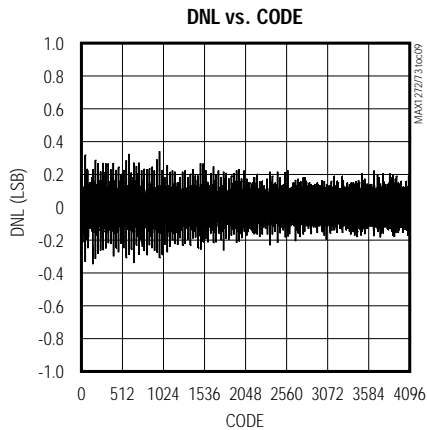
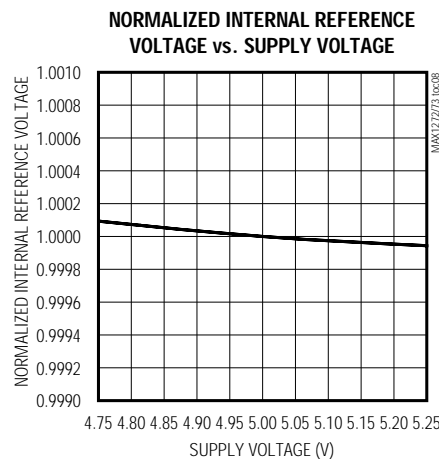
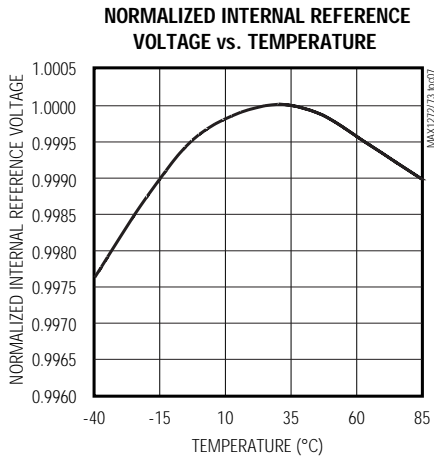
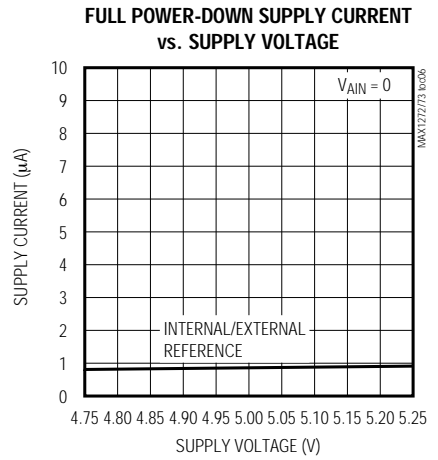
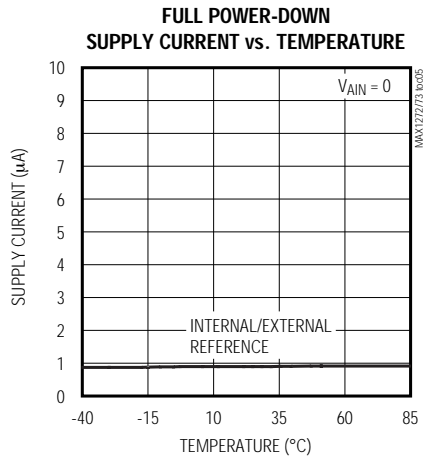
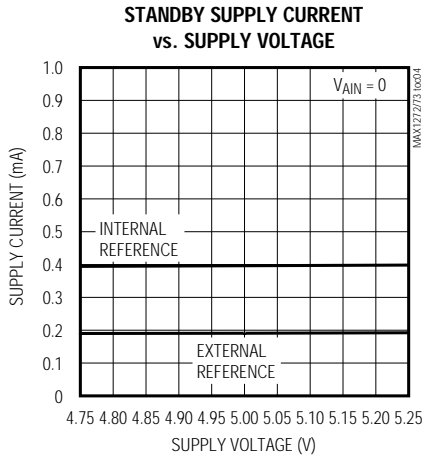
(Typical operating circuit, BIP = RNG = 1, $V_{DD} = 5V$, external reference mode, $V_{REF} = 4.096V$, $C_{REF} = 1.0\mu F$, $f_{SCLK} = 1.4MHz$, 50% duty cycle, 87ksps, $T_A = +25^\circ C$, unless otherwise noted.)



Fault-Protected, 12-Bit ADCs with Software-Selectable Input Range

Typical Operating Characteristics (continued)

(Typical operating circuit, BIP = RNG = 1, $V_{DD} = 5V$, external reference mode, $V_{REF} = 4.096V$, $C_{REF} = 1.0\mu F$, $f_{SCLK} = 1.4MHz$, 50% duty cycle, $T_A = +25^\circ C$, unless otherwise noted.)

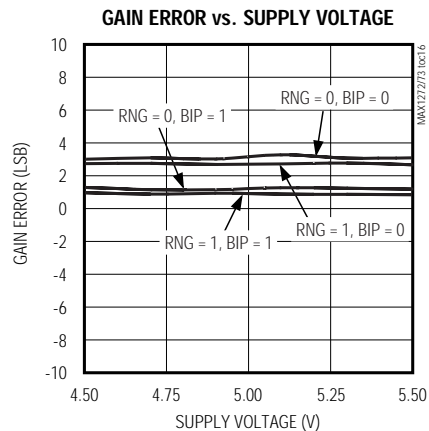
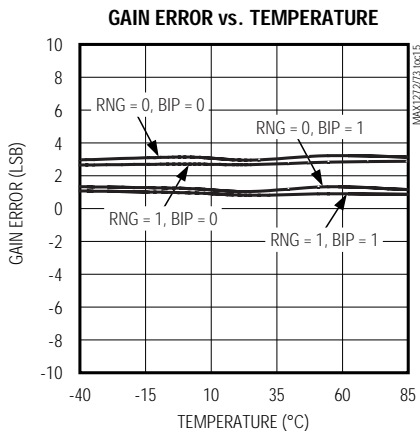
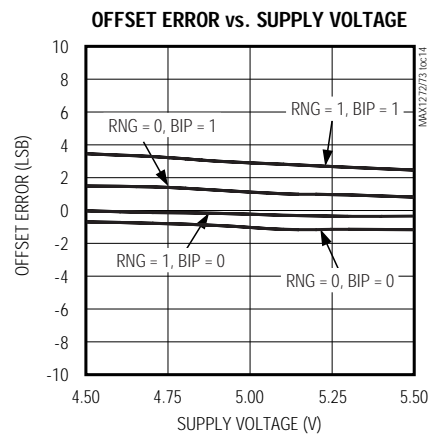
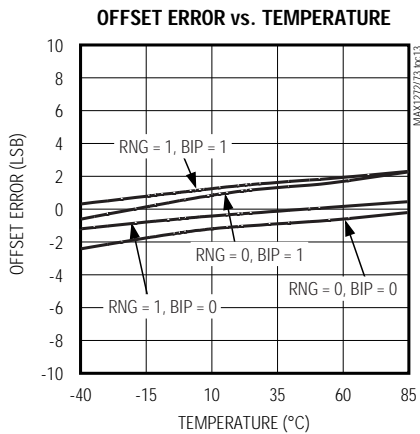
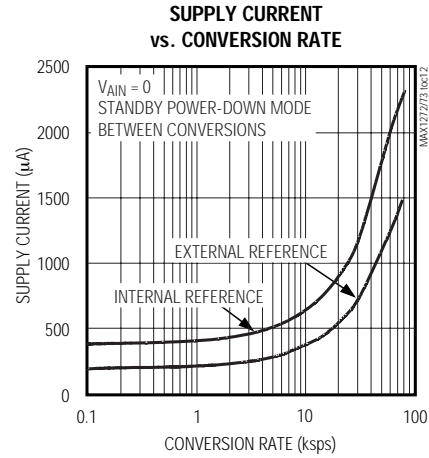
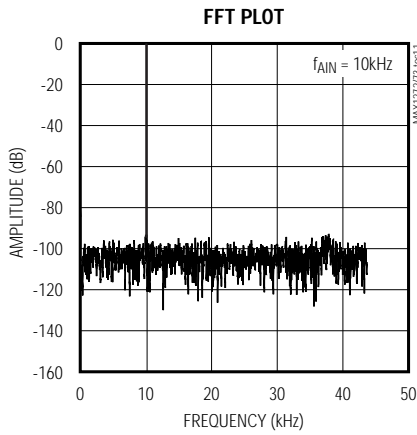


Fault-Protected, 12-Bit ADCs with Software-Selectable Input Range

MAX1272/MAX1273

Typical Operating Characteristics (continued)

(Typical operating circuit, BIP = RNG = 1, $V_{DD} = 5V$, external reference mode, $V_{REF} = 4.096V$, $C_{REF} = 1.0\mu F$, $f_{SCLK} = 1.4MHz$, 50% duty cycle, 87ksps, $T_A = +25^\circ C$, unless otherwise noted.)



Fault-Protected, 12-Bit ADCs with Software-Selectable Input Range

Pin Description

| PIN | NAME | FUNCTION |
|-----|------------------------|---|
| 1 | SCLK | Serial Clock Input. Clocks data in and out of serial interface. SCLK sets the conversion speed. |
| 2 | DIN | Serial Data Input. Data clocks in on the rising edge of SCLK. |
| 3 | V _{DD} | 5V Supply. Bypass with a 0.1μF capacitor to GND. |
| 4 | GND | Ground |
| 5 | AIN | Analog Input |
| 6 | REF | Reference Buffer Output/Reference Input. Bypass REF with a 1μF capacitor to GND. In internal reference mode, the reference buffer provides a 4.096V nominal output. For external reference mode, disable the internal reference buffer through the serial interface and apply an external reference to REF. |
| 7 | $\overline{\text{CS}}$ | Active-Low Chip-Select Input. Drive $\overline{\text{CS}}$ low to clock data into the MAX1272/MAX1273. See the <i>Input Data Format</i> section. |
| 8 | DOUT | Serial Data Output. Data clocks out on the falling edge of SCLK. DOUT is high impedance when $\overline{\text{CS}}$ is high. |

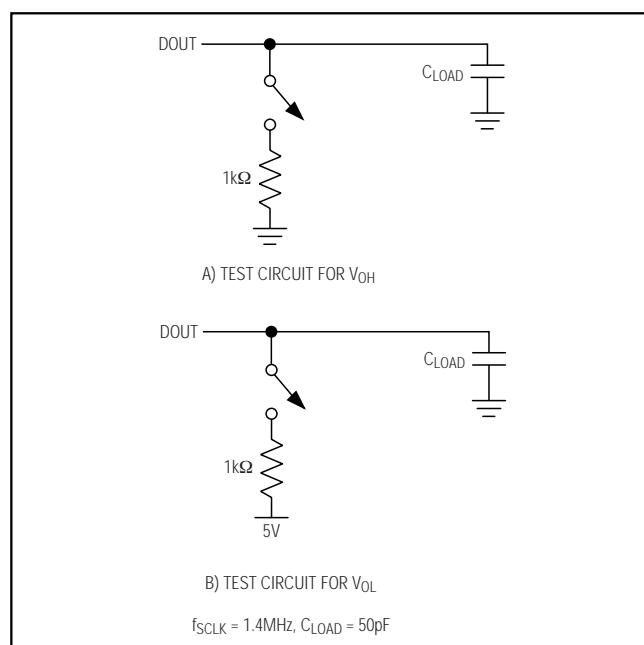


Figure 1. Output Load Circuit for Timing Characteristics

Detailed Description

Converter Operation

The MAX1272/MAX1273 multirange ADCs use successive approximation and internal track/hold (T/H) circuitry

to convert an analog signal to a 12-bit digital output. Figure 2 shows a block diagram of the MAX1272/MAX1273.

Analog-Input Track/Hold

The T/H tracking/acquisition mode begins on the falling edge of the fourth clock cycle in the 8-bit input control word and enters hold/conversion mode on the falling edge of the eighth clock cycle.

The MAX1272/MAX1273 input architecture includes a resistor-divider and a T/H system (Figure 3). When operating in bipolar or unipolar mode, the resistor-divider network formed by R1, R2, and R3 scales the signal applied at the input channel. Use a low source impedance (<4Ω) to minimize gain error.

Input Bandwidth

The ADC's small-signal input bandwidth depends on the selected input range and varies from 1.25MHz to 5MHz (see the *Electrical Characteristics*). The maximum sampling rate for the MAX1272/MAX1273 is 87ksps (16 clocks per conversion). Use undersampling techniques to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate.

Use anti-alias filtering to avoid the aliasing of high-frequency signals into the frequency band of interest. An anti-aliasing filter must limit the input bandwidth to no more than one half of the sampling frequency.

Fault-Protected, 12-Bit ADCs with Software-Selectable Input Range

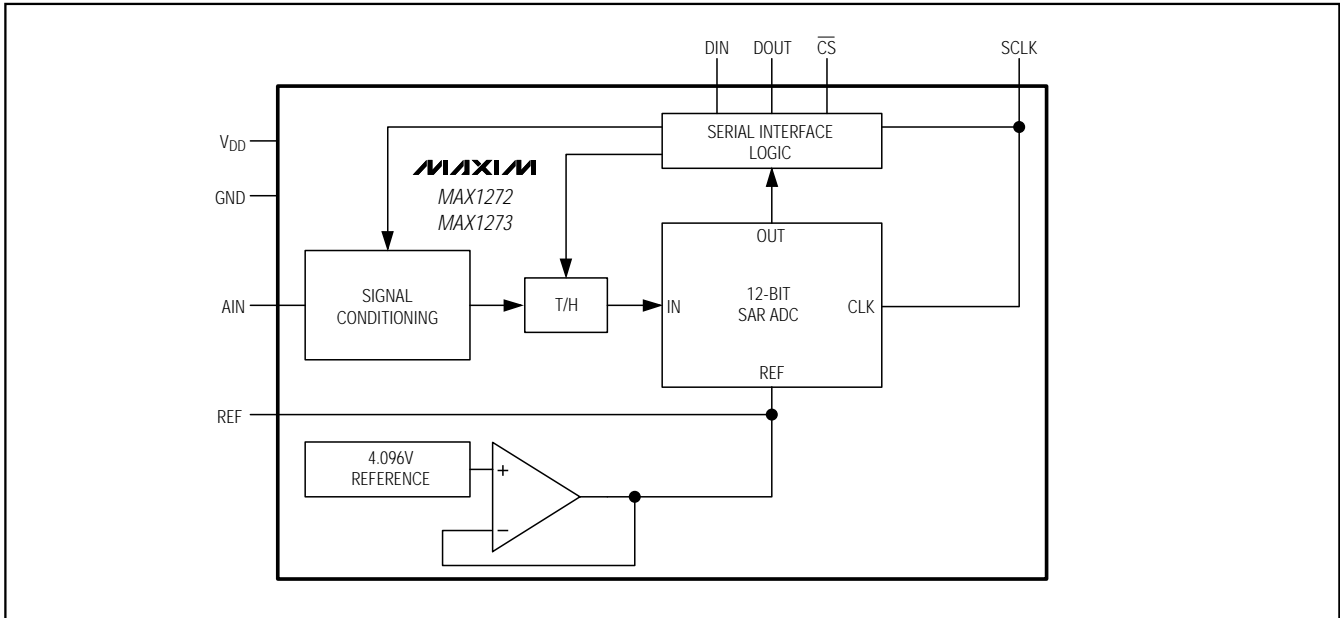


Figure 2. Simplified Block Diagram

Table 1. Control-Byte Format

| BIT 7 (MSB) | BIT 6 | BIT 5 | BIT 4 | Bit 3 | BIT 2 | BIT 1 | BIT 0 (LSB) |
|-------------|------------------------|---|------------------------|-------|-------|----------|-------------|
| START | RNG | BIP | $\overline{\text{PD}}$ | MODE1 | MODE0 | RESERVED | REF |
| BIT | NAME | DESCRIPTION | | | | | |
| 7 (MSB) | START | Write a logic 1 (see the <i>Input Data Format</i> section) | | | | | |
| 6 | RNG | Selects the full-scale input voltage range (Tables 2, 3) | | | | | |
| 5 | BIP | Selects unipolar or bipolar conversion mode (Tables 2, 3) | | | | | |
| 4 | $\overline{\text{PD}}$ | Selects normal operation ($\overline{\text{PD}} = 1$) or power-down ($\overline{\text{PD}} = 0$) mode | | | | | |
| 3 | MODE1 | Selects standby power-down (STBYPD) or full power-down (FULLPD) mode (Table 4) | | | | | |
| 2 | MODE0 | Selects delayed or immediate power-down mode (Table 4) | | | | | |
| 1 | RESERVED | Write a logic 0 | | | | | |
| 0 (LSB) | REF | Selects external (REF = 0, default) or internal (REF = 1) reference mode | | | | | |

Input Range and Protection

The MAX1272/MAX1273 provide software-selectable analog input voltage ranges. Program the analog input to one of four ranges by setting the appropriate control bits (RNG, BIP) in the control byte (Table 1). The MAX1272 has selectable input voltage ranges extending to $\pm 10\text{V}$ ($\pm V_{\text{REF}} \times 2.4414$), while the MAX1273 has selectable input voltage ranges extending to $\pm V_{\text{REF}}$. Figure 3 shows the equivalent input circuit.

Overvoltage circuitry at the analog input provides $\pm 12\text{V}$ fault protection for the MAX1272. This circuit limits the current going into or out of the device to less than 2mA, providing an added layer of protection from momentary over/undervoltages at the analog input. The overvoltage protection activates when the device enters power-down mode or if $V_{\text{DD}} = 0$.

Fault-Protected, 12-Bit ADCs with Software-Selectable Input Range

Table 2. Input Range and Polarity Selection for MAX1272

| INPUT RANGE | RNG | BIP | NEGATIVE FULL SCALE | ZERO SCALE | FULL SCALE |
|-------------|-----|-----|--------------------------|------------|-------------------------|
| 0 to 5V | 0 | 0 | — | 0 | $V_{REF} \times 1.2207$ |
| $\pm 5V$ | 0 | 1 | $-V_{REF} \times 1.2207$ | 0 | $V_{REF} \times 1.2207$ |
| 0 to 10V | 1 | 0 | — | 0 | $V_{REF} \times 2.4414$ |
| $\pm 10V$ | 1 | 1 | $-V_{REF} \times 2.4414$ | 0 | $V_{REF} \times 2.4414$ |

Table 3. Input Range and Polarity Selection for MAX1273

| INPUT RANGE | RNG | BIP | NEGATIVE FULL SCALE | ZERO SCALE | FULL SCALE |
|--------------------|-----|-----|---------------------|------------|---------------|
| 0 to $V_{REF} / 2$ | 0 | 0 | — | 0 | $V_{REF} / 2$ |
| $\pm V_{REF} / 2$ | 0 | 1 | $-V_{REF} / 2$ | 0 | $V_{REF} / 2$ |
| 0 to V_{REF} | 1 | 0 | — | 0 | V_{REF} |
| $\pm V_{REF}$ | 1 | 1 | $-V_{REF}$ | 0 | V_{REF} |

Table 4. Power-Down Selection

| PD | MODE1 | MODE0 | MODE |
|----|-------|-------|--|
| 1 | X | X | Normal operation (ADCs always active). Automatically enters delayed standby power-down mode between conversions. |
| 0 | 0 | 0 | Delayed standby power-down mode. |
| | | 1 | Immediate standby power-down mode. |
| | 1 | 0 | Delayed full power-down mode. |
| | | 1 | Immediate full power-down mode. |

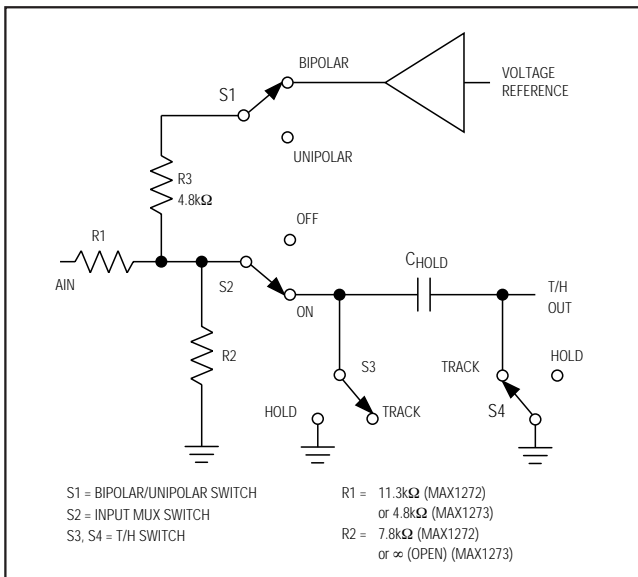


Figure 3. Equivalent Input Circuit

Input Data Format

Input data (control byte) clocks in at DIN on the rising edge of SCLK. \overline{CS} enables communication with the MAX1272/MAX1273. After \overline{CS} falls, the first arriving 1 represents the start bit (MSB) of the input control byte. The start bit is defined as follows:

- 1) The first high bit clocked into DIN with \overline{CS} low any time the converter is idle (e.g., after applying V_{DD}).
- 2) The first high bit clocked into DIN after bit 4 (D4) of a conversion in progress clocks out on DOUT.

See Table 1 for programming the control byte. Figure 4 shows the detailed serial interface timing.

Output Data Format

Output data (DOUT) clocks out MSB first on the falling edge of SCLK. The unipolar mode provides a straight binary output. The bipolar mode provides a two's complement binary output. For output binary codes, see the *Transfer Function* section.

Fault-Protected, 12-Bit ADCs with Software-Selectable Input Range

MAX1272/MAX1273

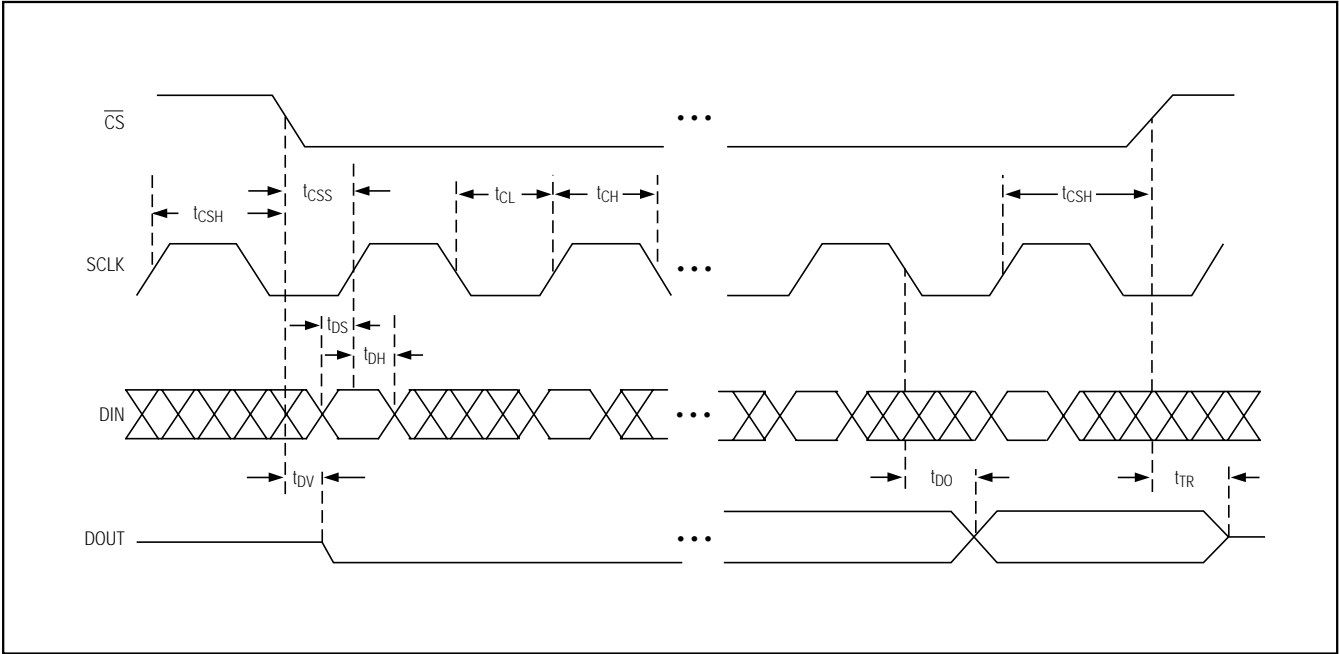


Figure 4. Detailed Serial Interface Timing

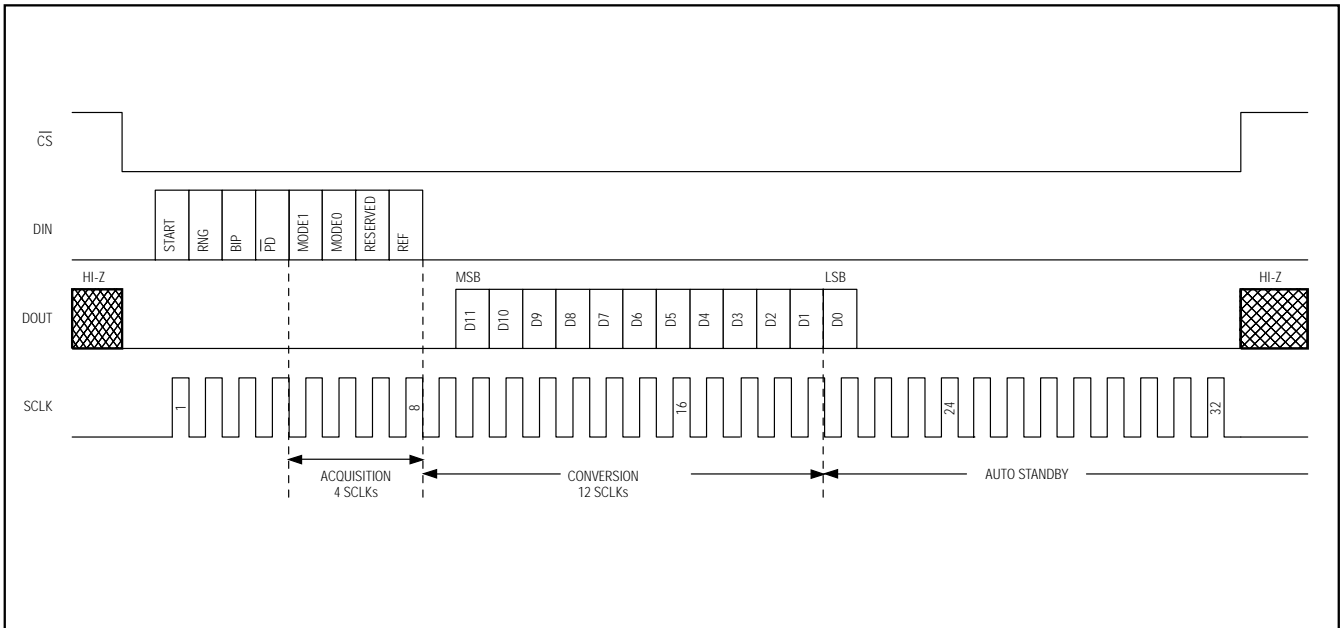


Figure 5. Conversion Timing, 21 Clocks/Conversion

Fault-Protected, 12-Bit ADCs with Software-Selectable Input Range

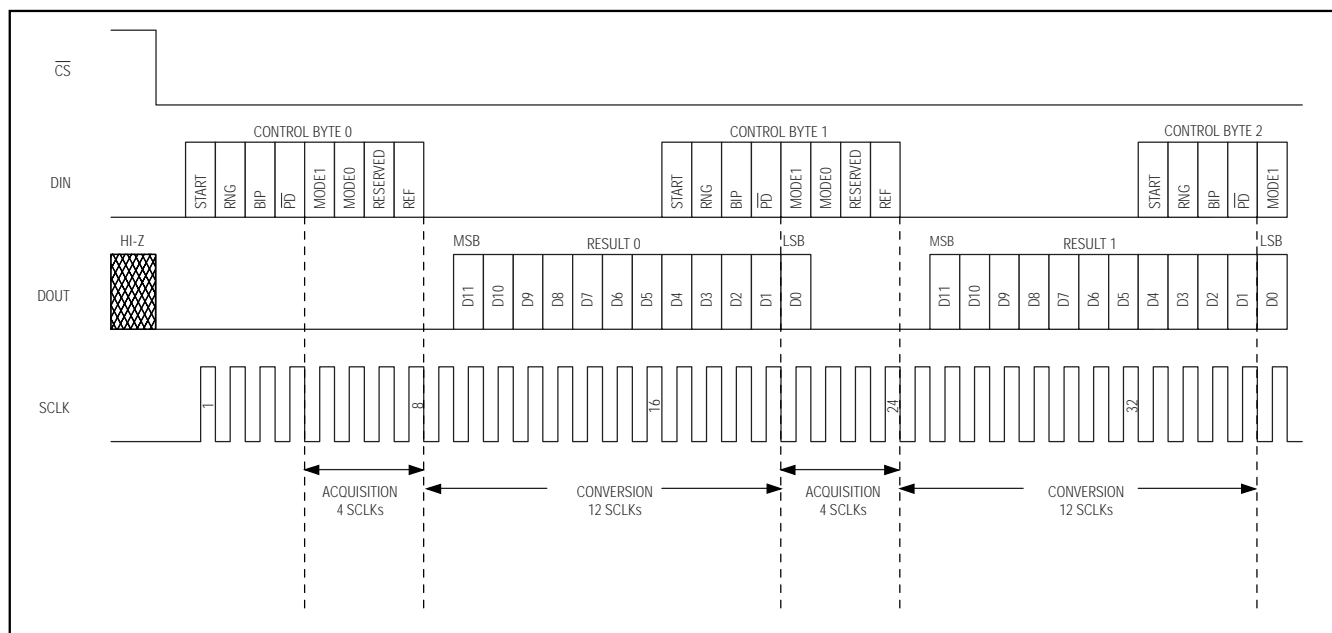


Figure 6. Conversion Timing, 16 Clocks/Conversion

Starting a Conversion

The MAX1272/MAX1273 use the serial clock to complete an acquisition. The falling edge of \overline{CS} does not start a conversion on the MAX1272/MAX1273. Each conversion requires a control byte. Programming the fourth bit in the control byte starts the acquisition sequence. Conversion starts on the falling edge of the eighth clock cycle after the start bit.

Keep \overline{CS} low during successive conversions. If a start bit is received after \overline{CS} transitions from high to low, but before the output bit 4 (D4) becomes available, the current conversion terminates and a new conversion begins. DOUT enters high-impedance state when \overline{CS} transitions high.

SCLK shifts data in and out of the MAX1272/MAX1273 and controls both acquisition and conversion timing. Conversion begins immediately after the end of the acquisition cycle. Successive-approximation bit decisions appear at DOUT on each of the following 12 clock falling edges (Figure 5). Additional clock falling edges result in trailing zeros at DOUT.

The maximum running rate of the MAX1272/MAX1273 is 16 clocks per conversion. A clock speed of 1.4MHz allows for a maximum sampling rate of 87ksps (Figure 6).

To achieve the maximum throughput, keep \overline{CS} low, and start the control byte after bit 4 (D4) of the conversion in progress clocks out on DOUT.

If \overline{CS} is low and SCLK is continuous, guarantee a start bit by first clocking in 16 zeros.

Applications Information

Power-On Reset

The MAX1272/MAX1273 power-up in normal operating mode (all internal circuitry active), and external reference mode. The MAX1272/MAX1273 require a start bit to initiate a conversion. The contents of the output data register clear during power-up.

Internal or External Reference

Operate the MAX1272/MAX1273 with an internal or an external reference. Configure REF as an internal reference output or an external reference input using the serial interface. When changing from external reference mode to internal reference mode, allow 2ms ($C_{REF} = 1\mu\text{F}$) for the reference to stabilize before taking any measurement.

Internal Reference

The internally trimmed reference provides 4.096V at REF. Bypass REF to GND with a 1.0 μF capacitor (Figure 7a).

Fault-Protected, 12-Bit ADCs with Software-Selectable Input Range

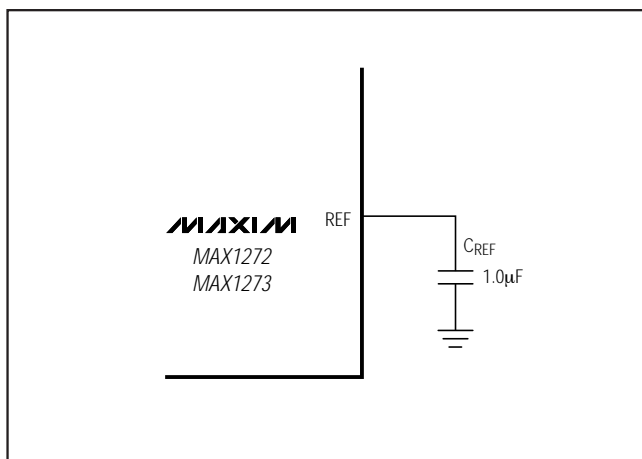


Figure 7a. Internal Reference Configuration

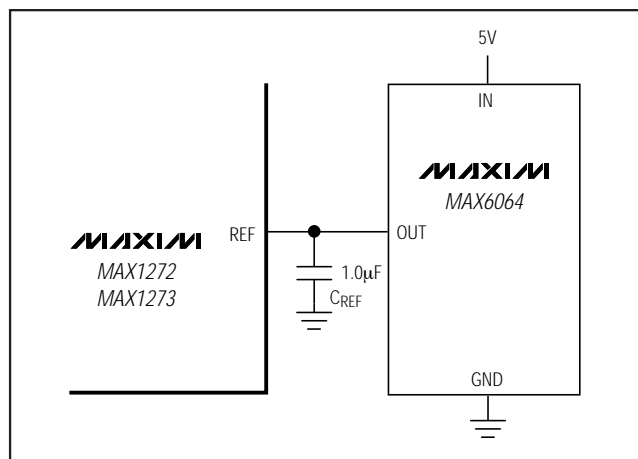


Figure 7b. External Reference Configuration

External Reference

To use an external reference, disable the internal buffer by setting the REF bit in the 8-bit control word to zero (see Table 1), and apply a reference voltage to REF. Use an external reference voltage ranging from 2.40V to 4.18V. External reference voltages less than 4.096V increase the ratio of RMS noise to the LSB value (full scale / 4096) resulting in performance degradation (loss of effective bits—ENOB).

The REF input impedance is a minimum of 4.8k Ω for DC currents; therefore, the external reference must be able to source 850 μ A during conversions and have an output impedance of less than 10 Ω . Bypass REF with a 1 μ F capacitor to GND as close to REF as possible (Figure 7b).

Power-Down Modes

To save power, configure the ADC for a low-current shutdown mode by setting the $\overline{\text{PD}}$ bit in the control byte. The MAX1272/MAX1273 features four programmable power-down modes: delayed standby power-down, immediate standby power-down, delayed full power-down, and immediate full power-down. Select standby or full power-down by programming MODE1 in the input control byte (Table 4). Select delayed or immediate power-down by programming MODE0 in the input control byte. Use the MODE0 bit to choose when the part enters the power-down state. For example, when MODE0 of the control byte is 0, the device remains powered up until after the current conversion ends (Figure 8). On the other hand, if MODE0 = 1, the device powers down on the falling edge of the eighth

serial clock cycle and no conversion takes place (Figure 9). In all power-down modes, the interface remains active with the conversion results available at DOUT. Additionally, the input overvoltage protection remains active in all power-down modes (MAX1272).

The first high bit on DIN after $\overline{\text{CS}}$ falls (start condition) powers up the MAX1272/MAX1273 from any software-selected power-down condition. With external reference mode, device power-up time from full power-down is typically 10 μ s. Send a control byte and allow 10 μ s for the device to wake up from full power-down. The next received control byte initiates a conversion.

When in internal reference mode, full power-down mode disables the internal reference and reference buffer. Only the interface circuitry remains active for reading conversion results. Send a control byte and allow 2ms ($C_{\text{REF}} = 1\mu\text{F}$) for the internal reference to settle and the MAX1272/MAX1273 to wake up from full power-down mode. The next received control byte initiates a conversion.

AutoShutdown™

The MAX1272/MAX1273 automatically enter standby power-down mode after each conversion without requiring any startup time on the next conversion.

Digital Interface

The MAX1272/MAX1273 feature a fully compatible SPI/QSPI and MICROWIRE serial interface. For SPI and QSPI, clear CPOL and CPHA in the microcontroller's SPI control registers.

AutoShutdown is a trademark of Maxim Integrated Products, Inc.

Fault-Protected, 12-Bit ADCs with Software-Selectable Input Range

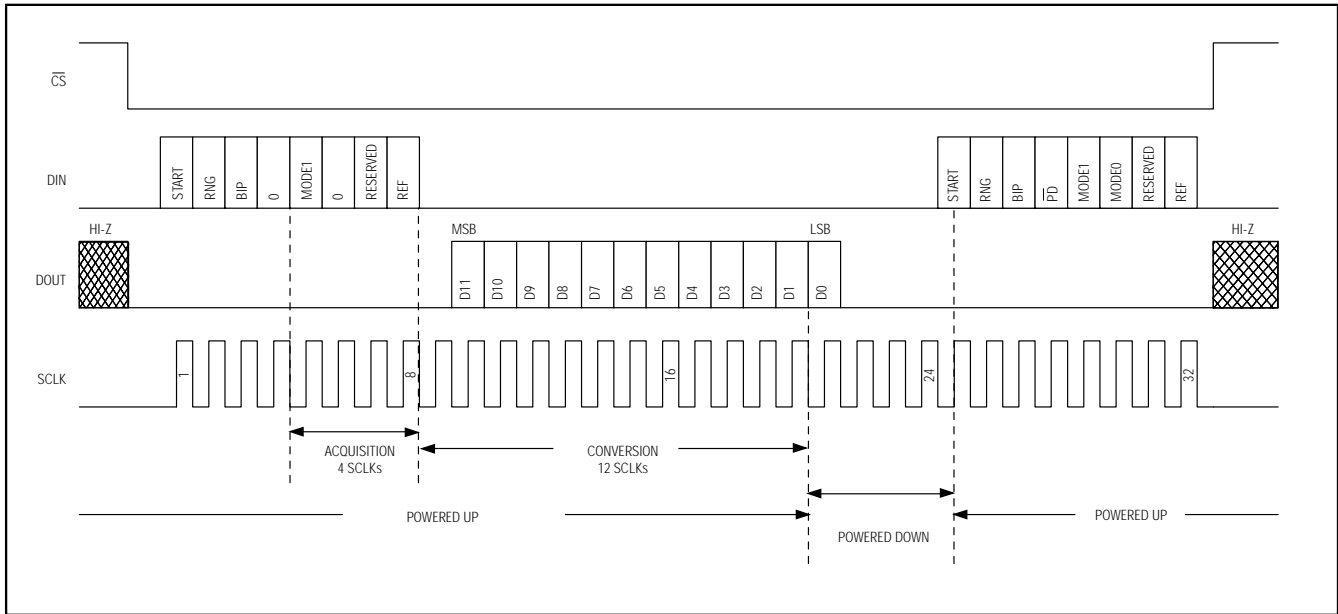


Figure 8. Delayed Power-Down Timing

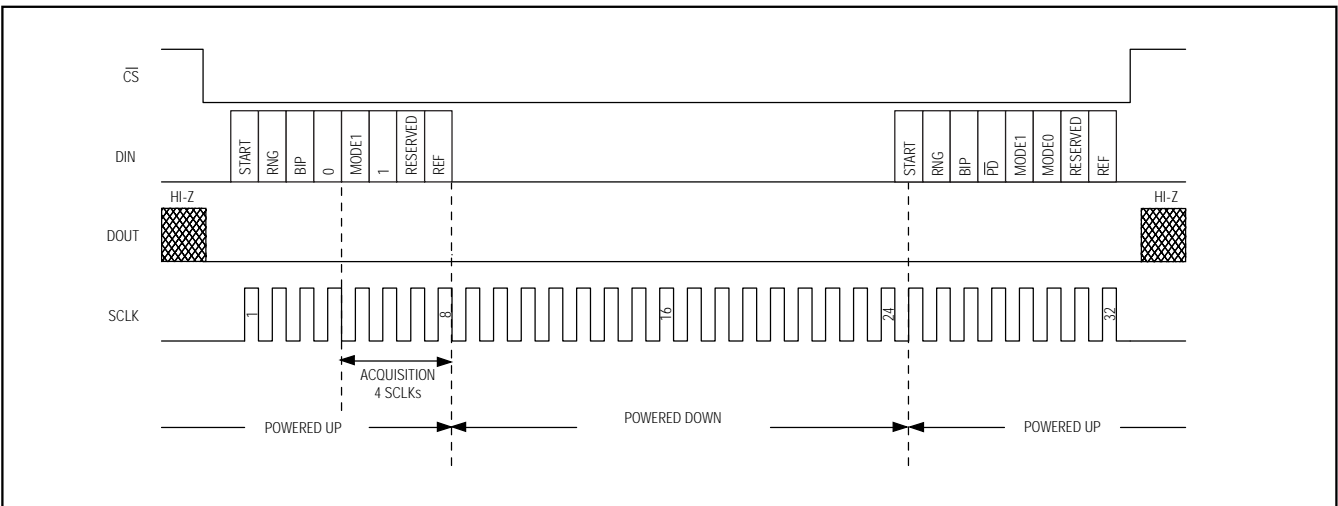


Figure 9. Immediate Power-Down Timing

SPI and MICROWIRE Interface

When using the SPI (Figure 10a) or MICROWIRE (Figure 10b) interfaces, set CPOL = 0 and CPHA = 0 in the SPI master. Conversion begins with a falling edge on \overline{CS} . Three consecutive 8-bit readings are necessary to obtain the entire 12-bit result from the ADC. DOUT data transitions on the serial clock's falling edge. The first 8-

bit data stream contains all leading zeros. The second 8-bit data stream contains a leading zero followed by the MSB through D5. The third 8-bit data stream contains D4–D0 followed by trailing zeros.

Fault-Protected, 12-Bit ADCs with Software-Selectable Input Range

QSPI Interface

Using the high-speed QSPI interface with CPOL = 0 and CPHA = 0, the MAX1272/MAX1273 support a maximum f_{SCLK} of 1.4MHz. Figure 11 shows the MAX1272/MAX1273 connected to a QSPI master.

PIC16 with SSP Module and PIC17 Interface

The MAX1272/MAX1273 are compatible with a PIC16/PIC17 controller (μC) using the synchronous serial-port (SSP) module.

To establish SPI communication, connect the controller as shown in Figure 12 and configure the PIC16/PIC17 as system master by initializing its synchronous serial-port control register (SSPCON) and synchronous serial-port status register (SSPSTAT) to the bit patterns shown in Tables 5 and 6.

In SPI mode, the PIC16/PIC17 μCs allow 8 bits of data to be transmitted and received simultaneously. Three consecutive 8-bit readings are necessary to obtain the entire 12-bit result from the ADC. DOUT data transitions on the serial clock's falling edge and is clocked into the

μC on SCLK's rising edge. The first 8-bit data stream contains all zeros. The second 8-bit data stream contains a leading zero followed by the MSB through D5. The third 8-bit data stream contains bits D4–D0 followed by trailing zeros.

Transfer Function

Output data coding for the MAX1272/MAX1273 is binary in unipolar mode with:

$$1\text{LSB} = \frac{FS}{4096}$$

and two's complement binary in bipolar mode with:

$$1\text{LSB} = \frac{2 \times |FS|}{4096}$$

Code transitions occur halfway between successive integer LSB values. Figures 13a and 13b show the input/output transfer functions for uni-polar and bipolar operations, respectively. For full-scale (FS) values, see Tables 2 and 3.

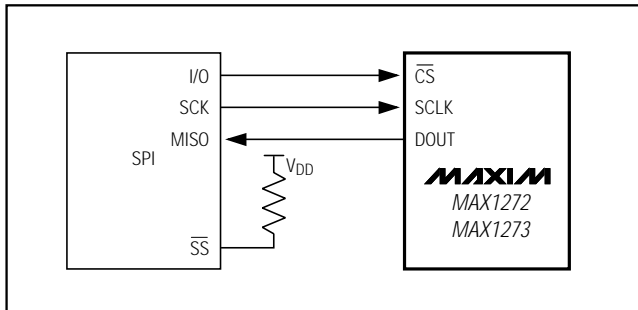


Figure 10a. SPI Connections

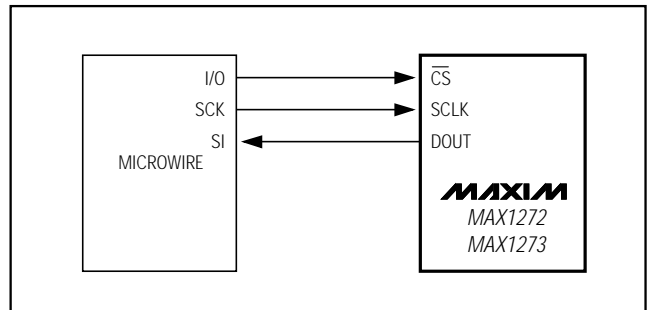


Figure 10b. MICROWIRE Connections

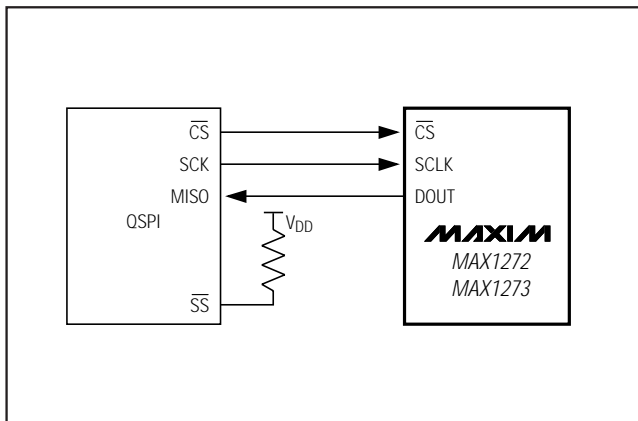


Figure 11. QSPI Connections

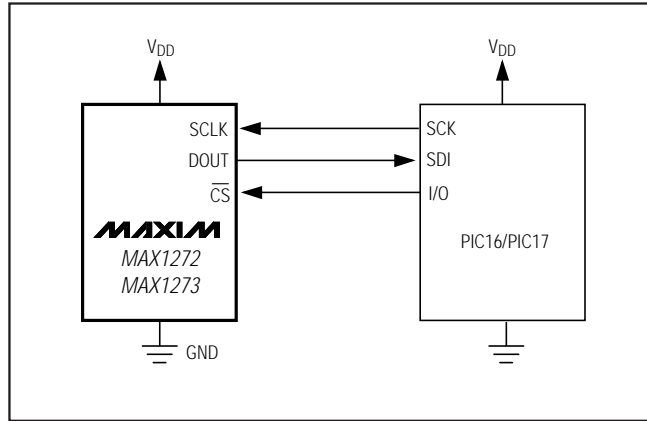


Figure 12. SPI Interface Connection for a PIC16/PIC17

Fault-Protected, 12-Bit ADCs with Software-Selectable Input Range

Table 5. Detailed SSPCON Register Contents—PIC16/PIC17

| CONTROL BIT | | | SYNCHRONOUS SERIAL-PORT CONTROL REGISTER (SSPCON) |
|-------------|------|---|---|
| WCOL | BIT7 | X | Write Collision Detection Bit |
| SSPOV | BIT6 | X | Receive Overflow Detection Bit |
| SSPEN | BIT5 | 1 | Synchronous Serial-Port Enable Bit: 0: Disables serial port and configures these pins as I/O port pins. 1: Enables serial port and configures SCK, SDO, and SCI pins as serial port pins. |
| CKP | BIT4 | 0 | Clock Polarity Select Bit. CKP = 0 for SPI master mode section. |
| SSPM3 | BIT3 | 0 | Synchronous Serial-Port Mode-Select Bit. Sets SPI master mode and selects $f_{CLK} = f_{OSC} / 16$. |
| SSPM2 | BIT2 | 0 | |
| SSPM1 | BIT1 | 0 | |
| SSPM0 | BIT0 | 1 | |

X = Don't care.

Table 6. Detailed SSPSTAT Register Contents—PIC16/PIC17

| CONTROL BIT | | | SYNCHRONOUS SERIAL-PORT STATUS REGISTER (SSPSTAT) |
|-------------|------|---|---|
| SMP | BIT7 | 0 | SPI Data Input Sample Phase. Input data is sampled at the middle of the data output time. |
| CKE | BIT6 | 1 | SPI Clock Edge-Select Bit. Data is transmitted on the rising edge of the serial clock. |
| D/A | BIT5 | X | Data Address Bit |
| P | BIT4 | X | Stop Bit |
| S | BIT3 | X | Start Bit |
| R/W | BIT2 | X | Read/Write Bit Information |
| UA | BIT1 | X | Update Address |
| BF | BIT0 | X | Buffer Full Status Bit |

X = Don't care.

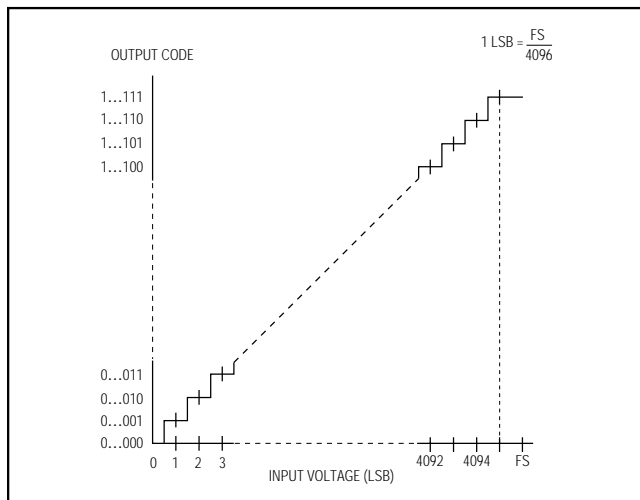


Figure 13a. Unipolar Transfer Function

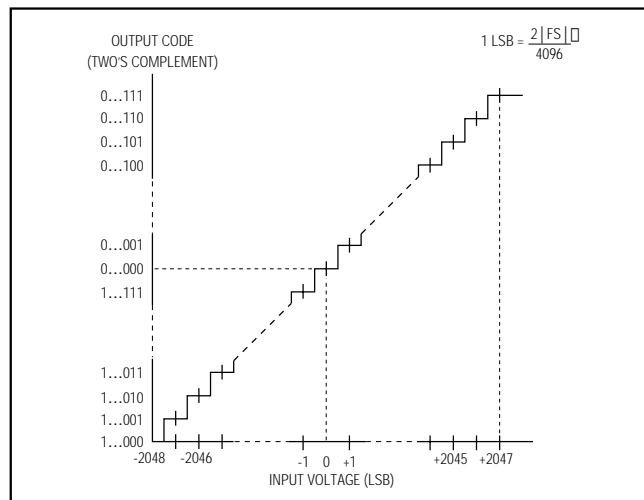


Figure 13b. Bipolar Transfer Function

Fault-Protected, 12-Bit ADCs with Software-Selectable Input Range

Layout, Grounding, and Bypassing

For best performance, use printed circuit (PC) boards. Wire-wrap configurations are not recommended since the layout should ensure proper separation of analog and digital traces. Do not run analog and digital lines parallel to each other, and do not lay out digital signal paths underneath the ADC package. Use separate analog and digital PC board ground sections with only one star point (Figure 14), connecting the two ground systems (analog and digital). For lowest-noise operation, ensure that the ground return to the star ground's power supply is low impedance and as short as possible. Route digital signals far away from sensitive analog and reference inputs.

High-frequency noise in the power supply (V_{DD}) can degrade the performance of the ADC's fast comparator. Bypass V_{DD} to the star ground with a $0.1\mu\text{F}$ capacitor located as close as possible to the MAX1272/MAX1273's power-supply input. Minimize capacitor lead length for best supply-noise rejection. Add an attenuation resistor (5Ω) to extremely noisy power supplies.

Definitions

Integral Nonlinearity

Integral nonlinearity (INL) is the deviation of the values on an actual transfer function from a straight line. This straight line can be either a best-straight-line fit or a line drawn between the endpoints of the transfer function, once offset and gain errors have been nullified. The static linearity parameters for the MAX1272/MAX1273 are measured using the endpoint method.

Differential Nonlinearity

Differential nonlinearity (DNL) is the difference between an actual step-width and the ideal value of 1 LSB. A DNL error specification of 1 LSB guarantees no missing codes and a monotonic transfer function.

Aperture Definitions

Aperture jitter (t_{AJ}) is the sample-to-sample variation in the time between samples. Aperture delay (t_{AD}) is the time between the falling edge of the sampling clock and the instant when the actual sample is taken.

Signal-to-Noise Ratio

For a waveform perfectly reconstructed from digital samples, signal-to-noise ratio (SNR) is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error).

The ideal, theoretical minimum analog-to-digital noise is caused by quantization noise error only and results directly from the ADC's resolution (N-bits):

$$\text{SNR} = (6.02 \times N + 1.76) \text{ dB}$$

In reality, there are other noise sources besides quantization noise: thermal noise, reference noise, clock jitter, etc. SNR is computed by taking the ratio of the RMS signal to the RMS noise, which includes all spectral components minus the fundamental, the first five harmonics, and the DC offset.

Signal-to-Noise Plus Distortion

Signal-to-noise plus distortion (SINAD) is the ratio of the fundamental input frequency's RMS amplitude to the RMS equivalent of all the other ADC output signals:

$$\text{SINAD (dB)} = 20 \times \log [\text{Signal}_{\text{RMS}} / (\text{Noise} + \text{Distortion})_{\text{RMS}}]$$

Effective Number of Bits

Effective number of bits (ENOB) indicates the global accuracy of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. With an input range equal to the full-scale range of the ADC, calculate the effective number of bits as follows:

$$\text{ENOB} = (\text{SINAD} - 1.76) / 6.02$$

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of the first five harmonics of the input signal to the fundamental itself. This is expressed as:

$$\text{THD} = 20 \times \log \left[\frac{\sqrt{(V_2^2 + V_3^2 + V_4^2 + V_5^2)}}{V_1} \right]$$

where V_1 is the fundamental amplitude and V_2 through V_5 are the 2nd- through 5th-order harmonics.

Spurious-Free Dynamic Range

Spurious-free dynamic range (SFDR) is the ratio of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next largest frequency component, excluding DC offset.

Fault-Protected, 12-Bit ADCs with Software-Selectable Input Range

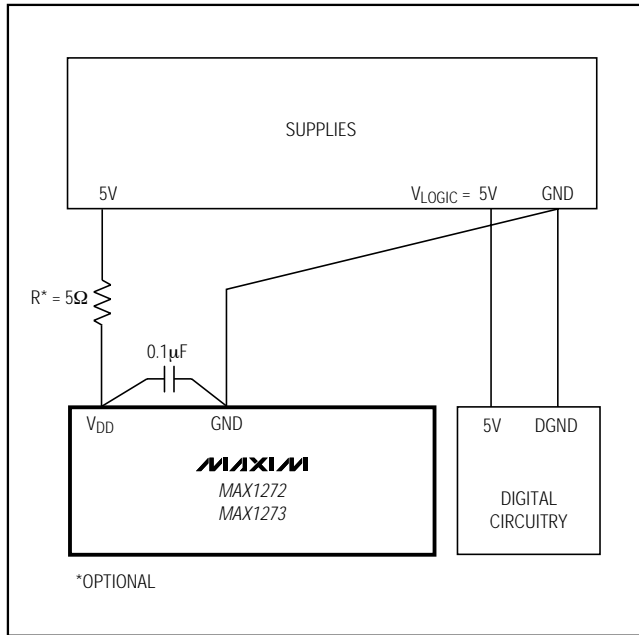
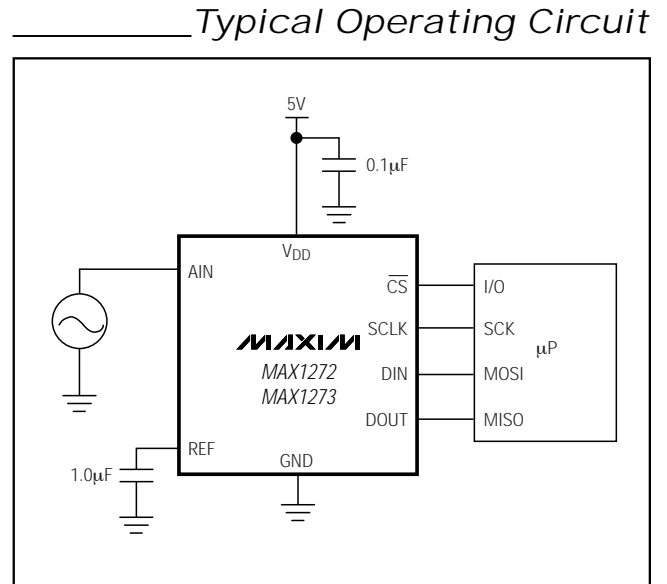


Figure 14. Power-Supply Grounding Connections



Chip Information

TRANSISTOR COUNT: 6146

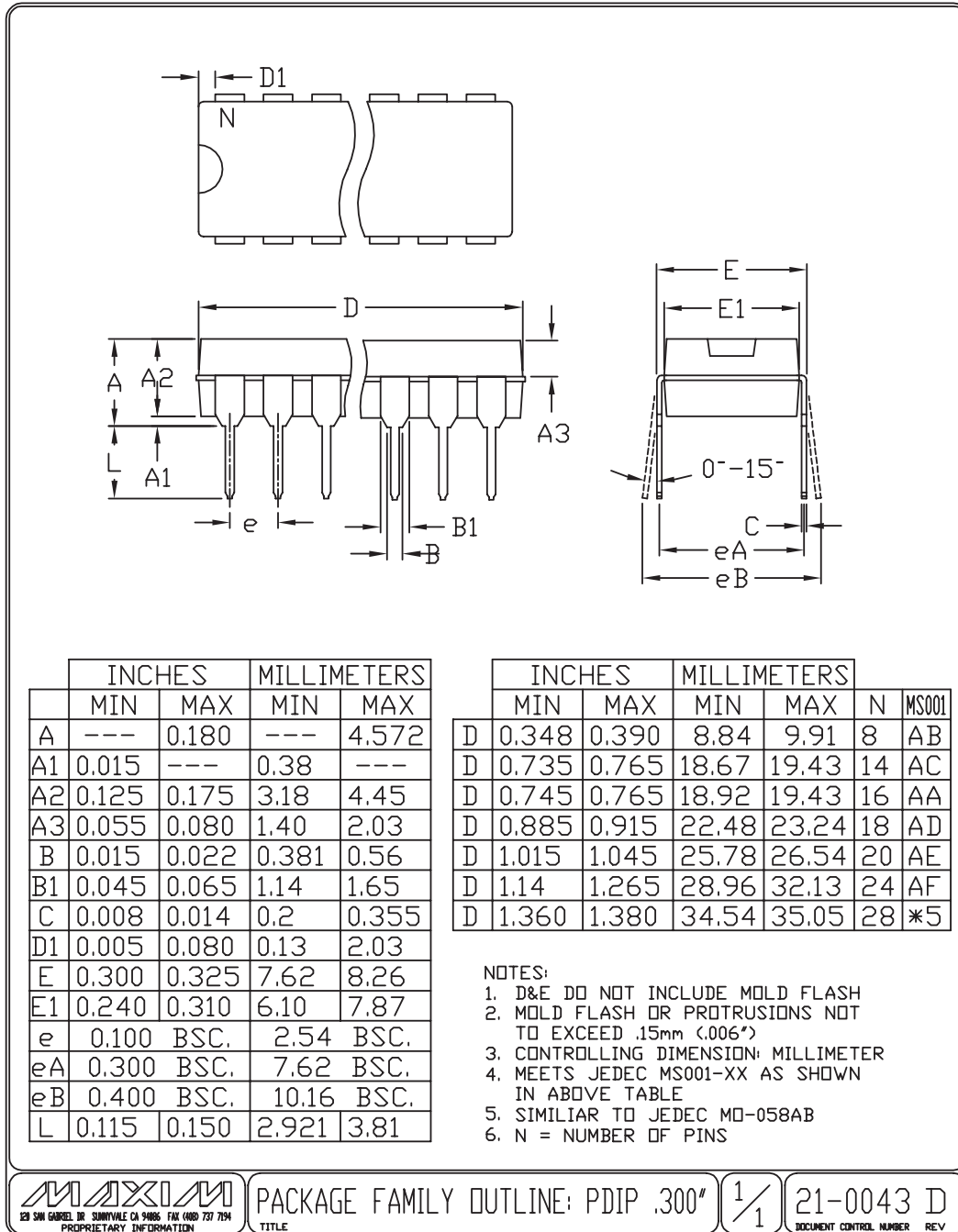
PROCESS: BiCMOS

Fault-Protected, 12-Bit ADCs with Software-Selectable Input Range

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

MAX1272/MAX1273



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